Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) A current conveyor circuit capable of operating at very low voltages, said current conveyor circuit comprising: ~~three LVCM's and four MOSFETS,~~

a port X for providing an input current;

a port Y for providing an input voltage;

a first low voltage current mirror (LVCM), LVCM1, having a first output port coupled to the port X and a second output port coupled to an output port Z;

a voltage buffer (VB) circuit, coupled between port X and port Y;

a second LVCM, LVCM2, coupled to the VB circuit, for maintaining constant drain currents of the VB circuit;

a third LVCM, LVCM3, coupled to the VB circuit, for maintaining a constant tail current in the VB circuit;

~~A~~ first and second MOSFETs, M3 and M4, respectively, with gates coupled together and further coupled to an output port of LVCM2;

a reference voltage provided to sources of M3 and M4, respectively;

first MOSFET M3 drain coupled to the port X and the first output port of LVCM1, LVCM1 providing a constant bias current to flow through M3; and

second MOSFET M4 drain coupled to the output port Z and the second output port of LVCM1.

~~wherein LVCM1 provides a constant bias current to flow through M3,~~

~~if port X is kept open and the difference between the bias current and the injected current flows through M3 if a current is injected into port X,~~

~~which gets reflected at port Z due to the action of LVCM1, M3 and M4,~~

~~LVCM2 maintains the drain currents of M1 and M2 constant, and~~

~~LVCM3 maintains a constant tail current in the circuit.~~

2. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 1, wherein the current conveyor circuit comprises of one PMOS LVCM.

3. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 1, wherein LVCM2 is a PMOS LVCM.

4. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 1, wherein the current conveyor circuit comprises of two NMOS LVCM's.

5. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 1, wherein LVCM1 is a single input, double output NMOS LVCM.

6. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 1, wherein LVCM2 is a single input, single output NMOS LVCM.

7. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 1, wherein each~~the~~ LVCM uses a~~the~~ conventional current mirror ~~CM~~ structure in conjunction with a level shifter transistor at its~~the~~ input port.

8. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 7~~1~~, wherein each~~the~~ LVCM imparts high swing capability.

9. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 8~~1~~, wherein the LVCM's ensure maximum possible input and output voltage swings, giving rise to rail to rail capability to voltage transfer blocks.

10. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 7~~1~~, wherein an adaptive biasing technique is used in each~~the~~ LVCM.

11. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 10, wherein the adaptive biasing technique increases the input voltage swing and decreases the offset current.

12. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 1, wherein the VB circuit comprises:

a first MOSFET, M1, having a first gate, a first source and a first drain, the first gate coupled to the port X, the first drain coupled to an input port of LVCM2, the first source coupled to an output port of LVCM3; and

a second MOSFET, M2, having a second gate, a second source and a second drain, the second gate coupled to the port Y, the second drain coupled to the output port of LVCM2, the second source coupled to the first source of M1 and further coupled to the output port of LVCM3,

wherein ~~MOSFET's~~ M1 and M2 form a differential pair.

13. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 12, wherein ~~the~~ voltage ~~at port voltage~~ at the port Y gets transferred to the port X due to an~~the~~ action of the differential pair.

14. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 12, wherein the current conveyor circuit ~~may~~ further comprises ~~of~~ a capacitance C connected between the first drain of M1 and second gate of M2.

15. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 14, wherein the capacitance is connected to provide compensation.

16. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 12, wherein the current conveyor circuit ~~may~~ further comprises ~~of~~ a resistance connected between the first and second gates ~~terminal~~ of M1 and M2, respectively.

17. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 16, wherein the resistance enhances the frequency response of the current conveyer circuit.

18. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 1, wherein the ~~MOSFET's~~ M3 and M4 form a current mirror.

19. (Currently Amended) ~~A~~The current conveyor circuit as claimed in claim 1, wherein the current conveyor circuit operates at a voltage range of ± 1V.

20. (New) The current conveyor circuit as claimed in claim 1, when the port X is open, LVCM1 provides the constant bias current to flow through M3.

21. (New) The current conveyor circuit as claimed in claim 20, wherein a current source is provided to the port X, for providing a difference current between the bias current and an injected current to flow through M3, the combination of LVCM1, M3 and M4 reflecting the difference current at the port Z.